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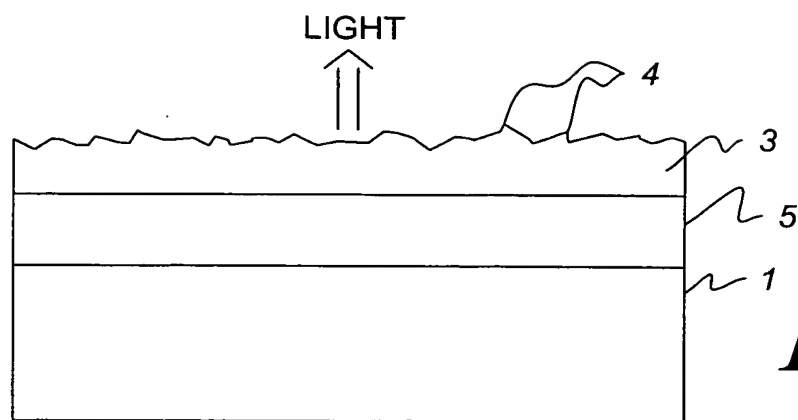


Fig. 1

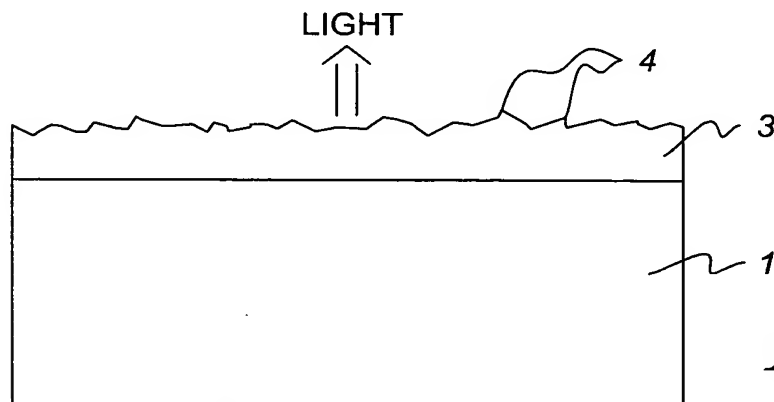


Fig. 2

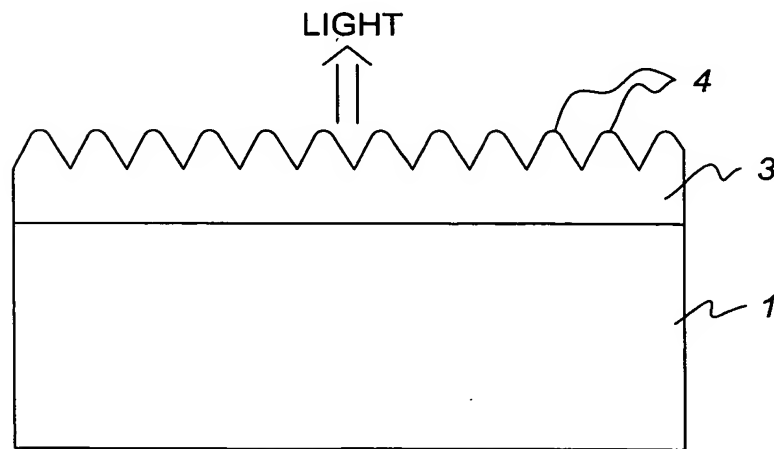


Fig. 3

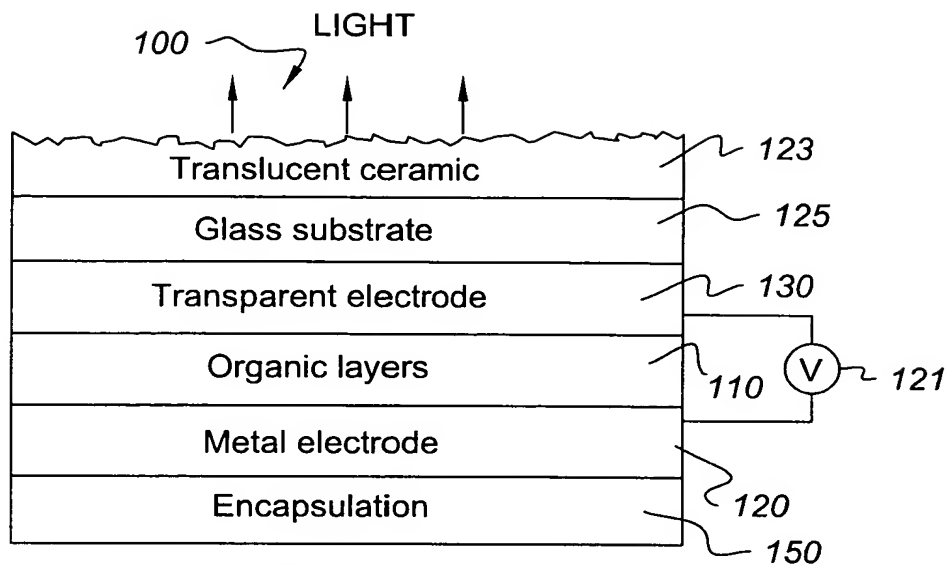


Fig. 4

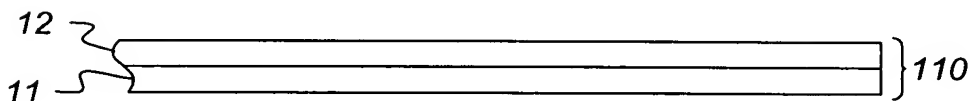


Fig. 5

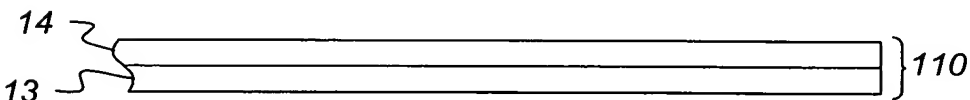


Fig. 6

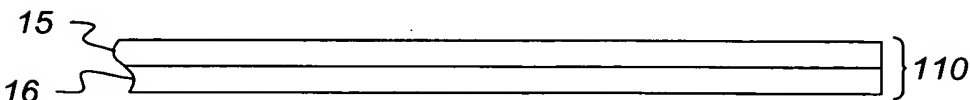


Fig. 7

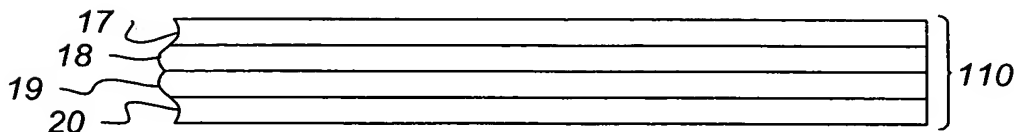


Fig. 8

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FIG. 1 is a cross-sectional view of a device 100. The device 100 includes a substrate 120. A top layer 125 is disposed on the substrate 120. A bottom layer 123 is disposed on the substrate 120. A central region 110 is defined by the top layer 125 and the bottom layer 123. A patterned layer 101 is disposed in the central region 110. A bottom layer 121 is disposed on the substrate 120. The bottom layer 121 is connected to a voltage source V via contacts 162 and 164. Arrows indicate light emission from the top surface of the device 100.

Fig. 9

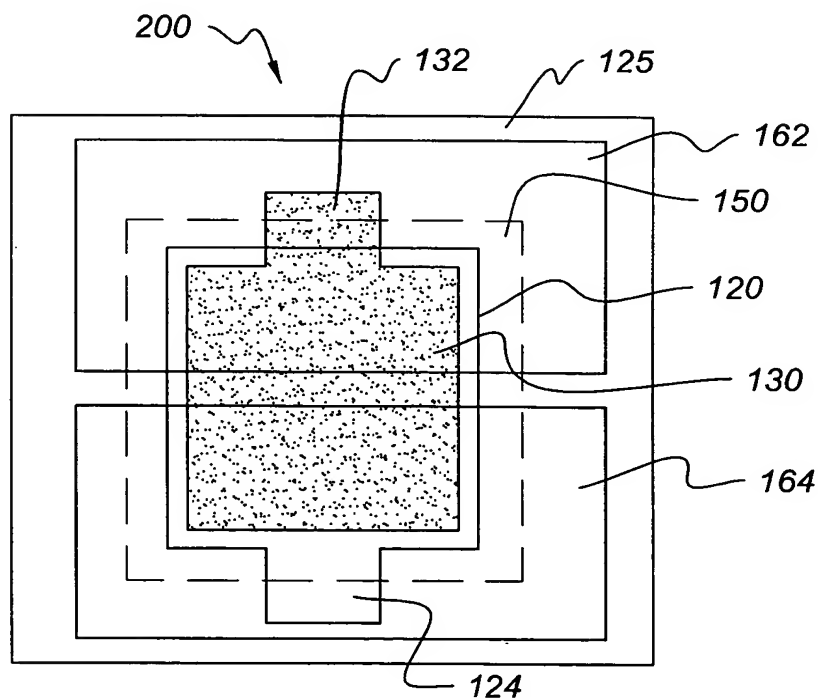


Fig 10

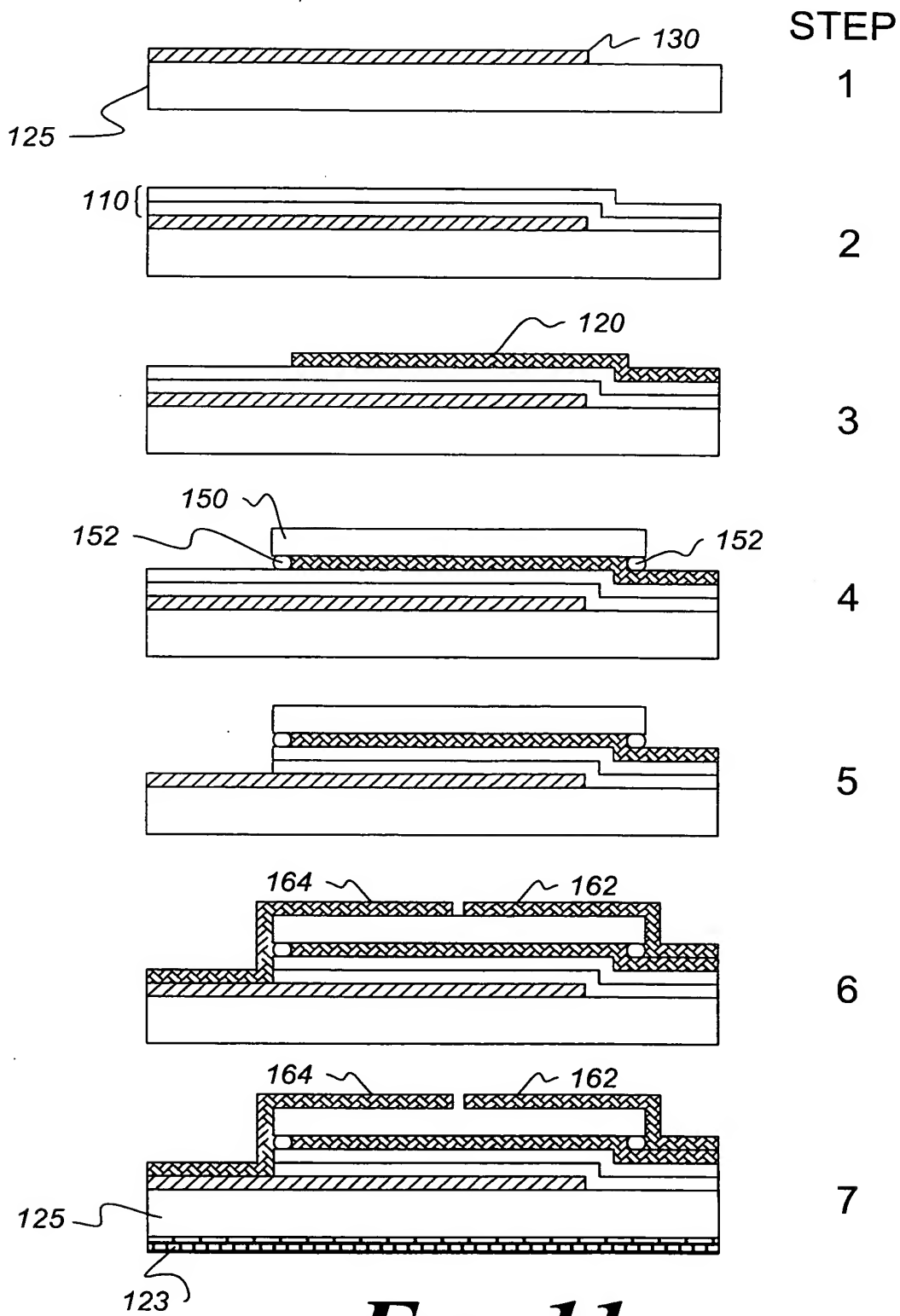


Fig 11

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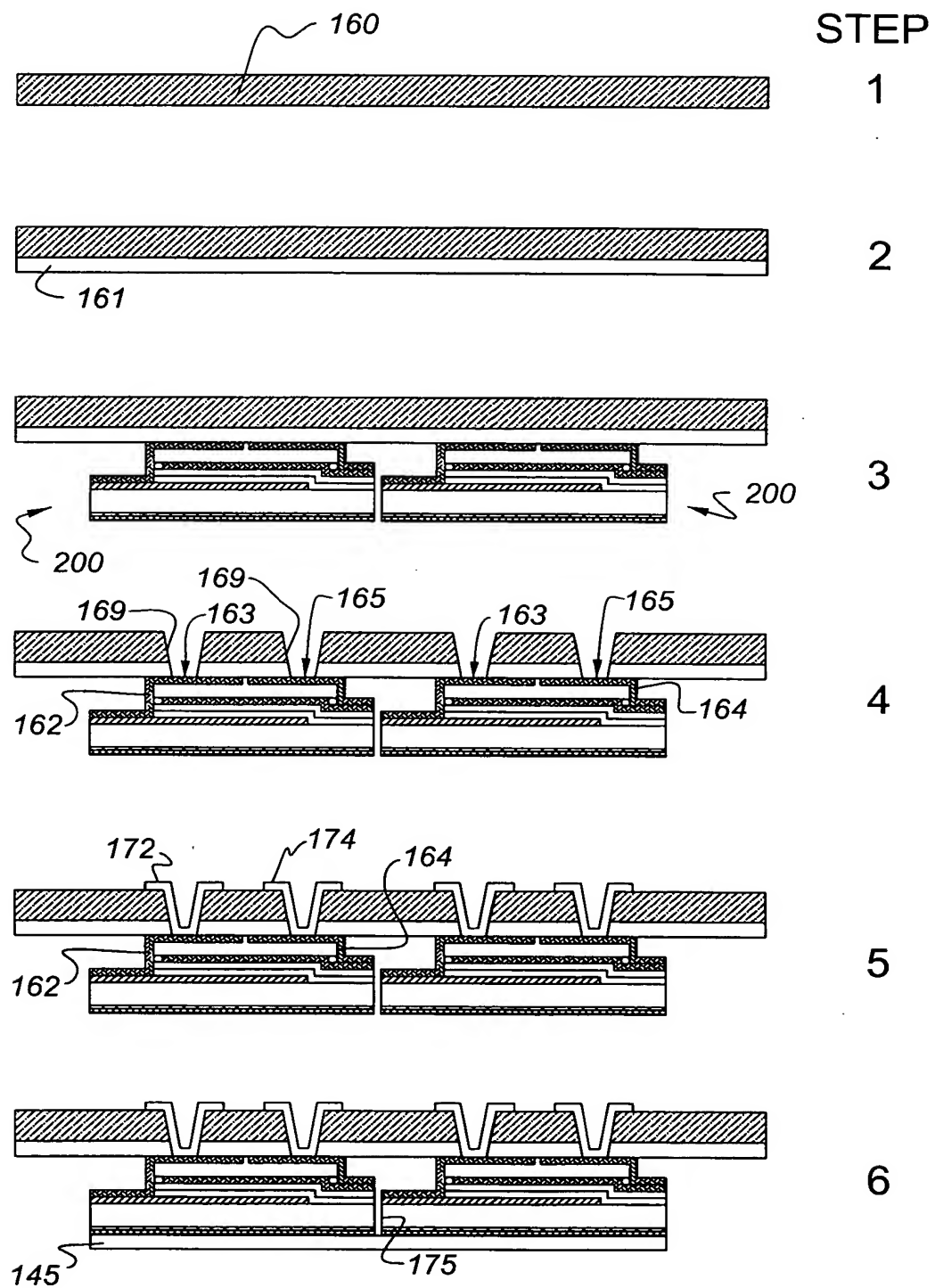


Fig. 12

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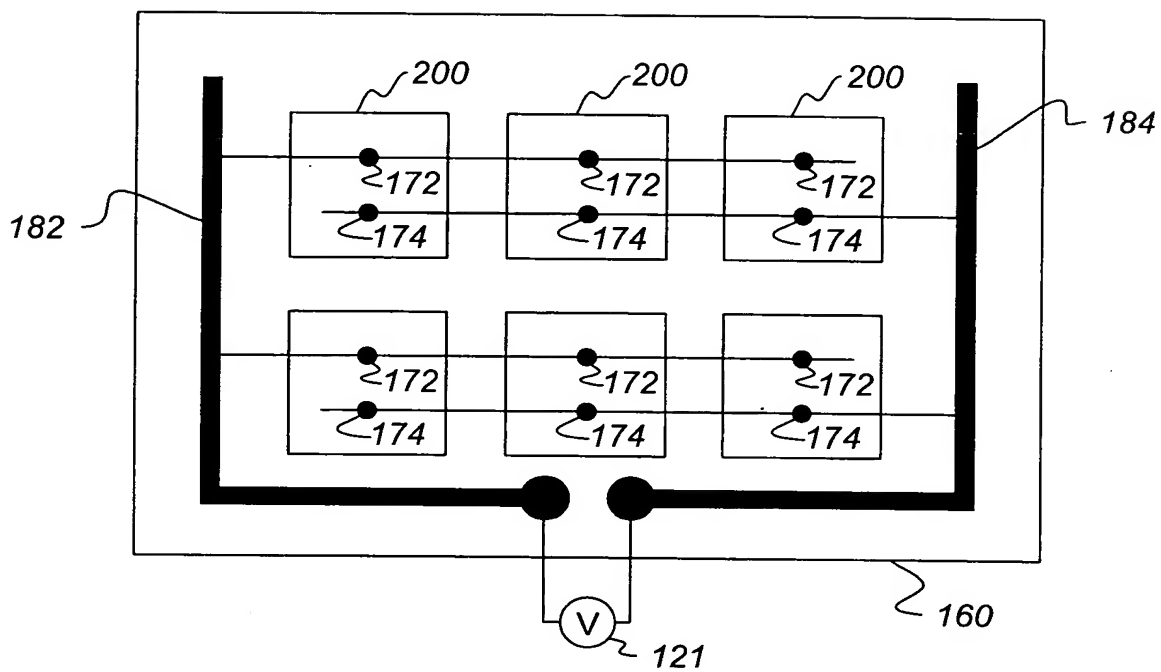


Fig. 13

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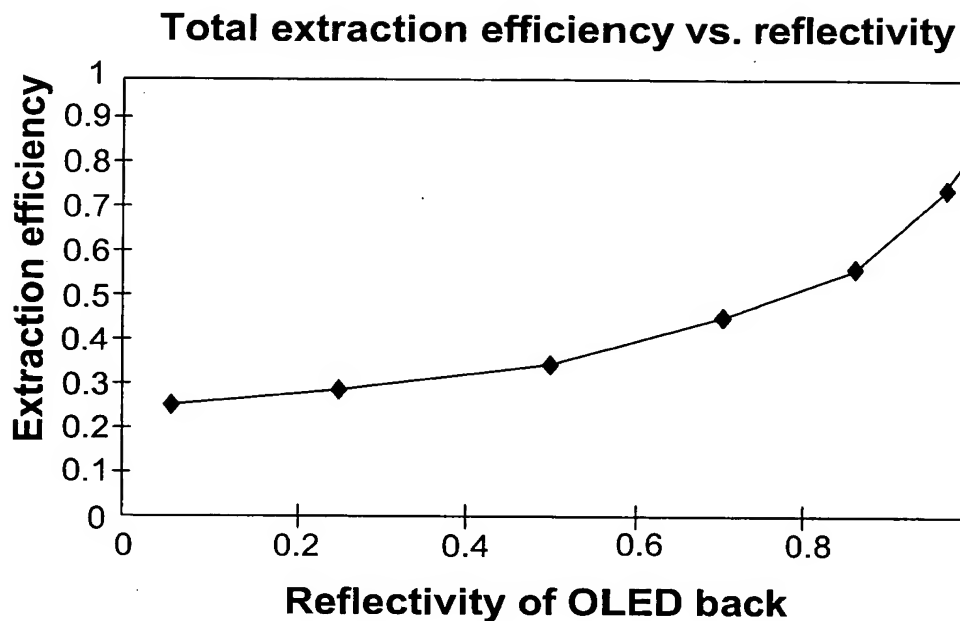


Fig. 14

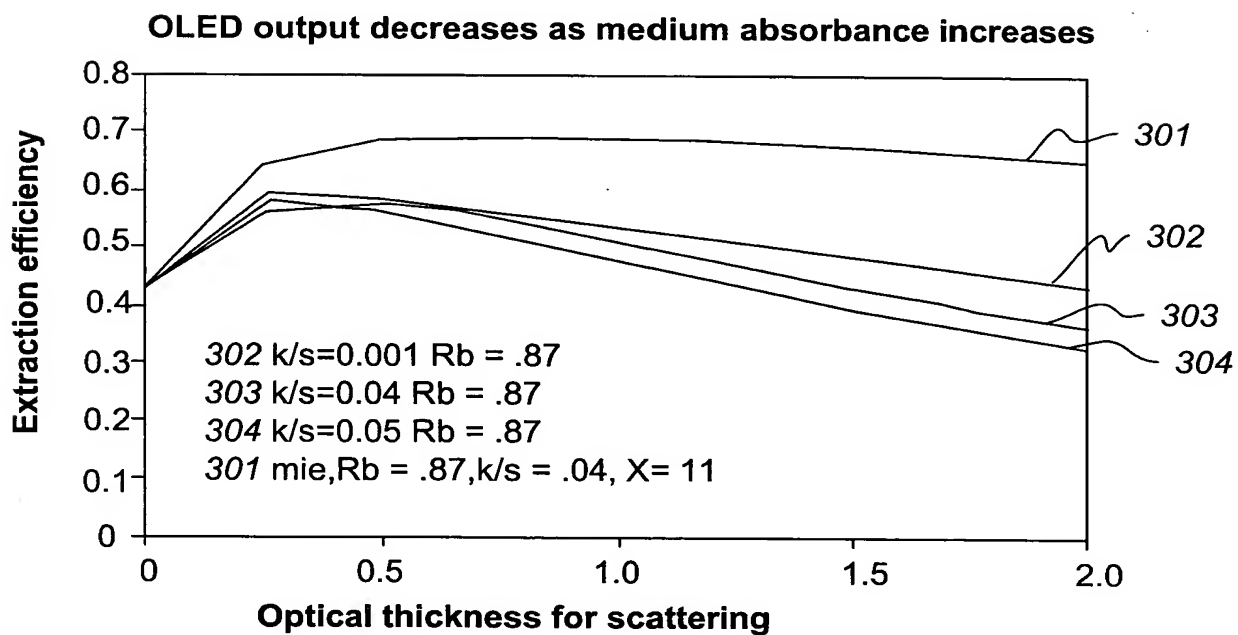
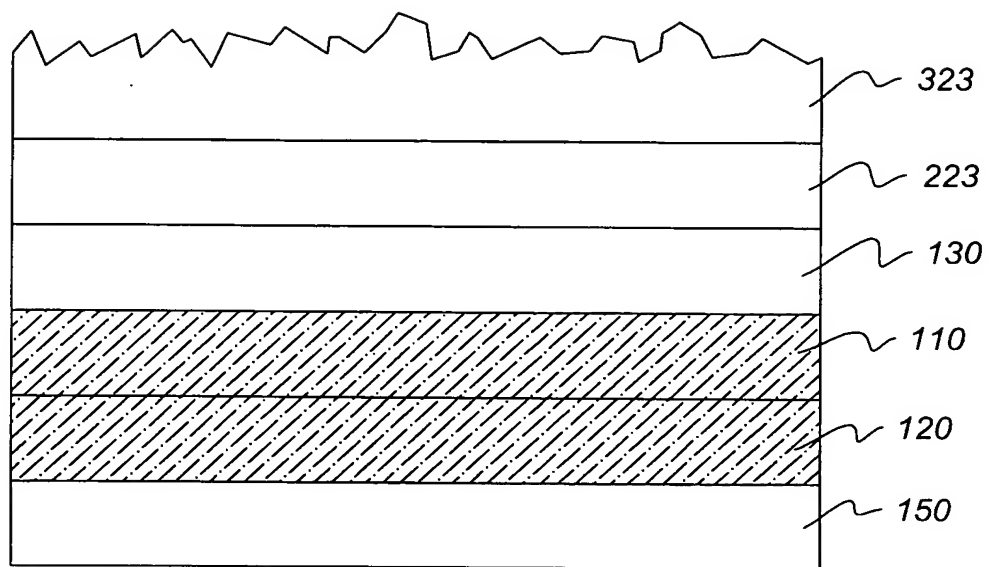


Fig. 15

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Fig. 16